REMARKS

Claims 1, 3, 4, 8, 9, 13, 14 and 18 are pending in the present application. Claims 1, 8, 13 and 18 have been amended. Claims 5, 6, 10-12 and 15-17 have been canceled.

Telephone Interview

Applicant acknowledges the courtesy extended by Examiner Trong Phan during the telephone interview conducted on November 1, 2007, and the assistance offered by Supervisor Amir Zarabian. During the telephone interview, Examiner Phan confirmed that all the objections to the drawings and specification, and all the claim rejections under 35 U.S.C. 112, second paragraph, as outstanding in the Final Office Action dated June 6, 2007, have been withdrawn.

Claim Rejections-35 U.S.C. 102

Claims 1, 3, 4, 8, 9, 12-14, 17 and 18, insofar as understood, have been rejected under 35 U.S.C. 102(b) as being anticipated by the Sakamoto reference (U.S. Patent No. 6,445,632). This rejection, insofar as it may pertain to the pending claims, is respectfully traversed for the following reasons.

The method of storing data of claim 1 includes in combination among other features "wherein the first bit line is connected to the first sense amplifier via a switching transistor, and wherein the switching transistor is driven to be on during a writing

operation by a first signal that changes between a ground level and a first voltage, and is then driven to be on after the writing operation by a second signal that changes between the ground level and a second voltage, the second voltage is higher than the first voltage". Applicant respectfully submits that the Sakamoto reference as relied upon does not disclose these features.

The Examiner has asserted at the top of page 12 of the current Office Action dated June 6, 2006, that the features of driving the switching transistor of claim 1 are met by signal øBUla that is shown in Figs. 2 and 3 of the Sakamoto reference. Signal øBUla drives transfer gates T2 of bit line isolation gates BGUa. However, as may be readily understood in view of Fig. 3 of the Sakamoto reference, signal øBUla merely changes between a low level and a single particular high level. Transfer gates T2 of bit line isolation gates BGUa of the Sakamoto reference are not driven to be on during a writing operation by a first signal that changes between a ground level and a first voltage, and are not then driven to be on after the writing operation by a second signal that changes between the ground level and a second voltage, whereby the second voltage is higher than the first voltage, as would be necessary to meet the features of claim 1. Applicant therefore respectfully submits that the method of storing data of claim 1 distinguishes over the Sakamoto reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1, 3 and 4, is improper for at least these reasons.

The method of storing data of claim 8 includes in combination among other

features "wherein the first data is transferred from the first sense amplifier to the first bit line via a switching transistor, wherein the switching transistor is driven during a writing operation by a first signal that changes between a ground level and a first voltage, and is then driven after the writing operation by a second signal that changes between the ground level and a second voltage, the second voltage is higher than the first voltage".

Applicant respectfully submits that the method of storing data of claim 8 distinguishes over the Sakamoto reference for at least somewhat similar reasons as noted above. Particularly, signal øBUla in Fig. 3 of the Sakamoto reference merely changes between a low level and a single particular high level. Transfer gates T2 of bit line isolation gates BGUa of the Sakamoto reference are not driven to be on during a writing operation by a first signal that changes between a ground level and a first voltage, and are not then driven to be on after the writing operation by a second signal that changes between the ground level and a second voltage, whereby the second voltage is higher than the first voltage, as would be necessary to meet the features of claim 8. Applicant therefore respectfully submits that the method of storing data of claim 8 distinguishes over the Sakamoto reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 8 and 9, is improper for at least these reasons.

The method of storing data of claim 13 includes in combination among other features "wherein the first data is transferred from the first sense amplifier to the first bit line via a switching transistor, wherein the switching transistor is driven by a first signal

that changes between ground level and a first voltage, and is then driven by a second signal that changes between the ground level and a second voltage, the second voltage is higher than the first voltage".

Applicant respectfully submits that signal øBUIa in Fig. 3 of the Sakamoto reference merely changes between a low level and a single particular high level. Transfer gates T2 of bit line isolation gates BGUa of the Sakamoto reference are not driven to be on by a first signal that changes between a ground level and a first voltage, and are not then driven to be on by a second signal that changes between the ground level and a second voltage, whereby the second voltage is higher than the first voltage, as would be necessary to meet the features of claim 13. Applicant therefore respectfully submits that the method of storing data of claim 13 distinguishes over the Sakamoto reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 13 and 14, is improper for at least these reasons.

The method of transferring data of claim 18 distinguishes over the Sakamoto reference for at least somewhat similar reasons as set forth above with respect to claim 13. Signal øBUIa in Fig. 3 of the Sakamoto reference merely changes between a low level and a single particular high level. Signal øBUIa clearly can not be interpreted as both the first and second signals of claim 18. Moreover, the Sakamoto et al. reference does not mention or consider voltage drop of a switching transistor responsive to respective first and second signals as featured in claim 18. Applicant therefore respectfully submits that the method of transferring data of claim 18 distinguishes over

the Sakamoto reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 18, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 5, 6, 10, 11, 15 and 16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sakamoto reference in view of the Kwon et al. reference (U.S. Patent No. 5,973,972). Although Applicant does not concede that this rejection is proper, claims 5, 6, 10, 11, 15 and 16 have been canceled, to advance prosecution of this application. The Examiner is therefore respectfully requested to withdraw this rejection.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to November 6, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $460.00

should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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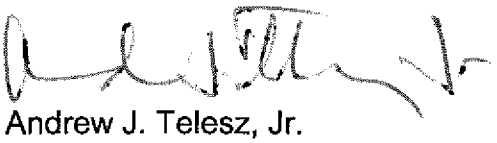

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